UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,927,413 B2
APPLICATION NO. : 10/717375
DATED : August 9, 2005
INVENTOR(S) : Mears et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

The title page should be deleted to appear as per attached title page.

The illustrated figure 1 should be deleted and new figure 1 inserted.

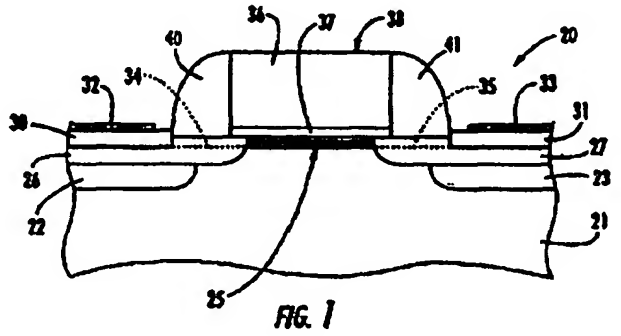

FIG. 1

Column 1, Line 42	Delete: "on a binary" Insert: --on binary--
Column 1, Line 66	Delete "in a silicon" Insert: --in silicon--
Column 1, Line 67	Delete: "electromuminescence" Insert: --electroluminescence--
Column 3, Line 4	Delete: "as may" Insert: --as may be--
Column 5, Line 11	Delete: "gate 35" Insert: --gate 38--
Column 5, Line 60	Delete: "gate 35" Insert: --gate 38--
Column 7, Line 63	Delete: "from the both" Insert: --from both--

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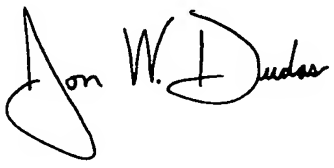
Column 9, Lines 44-46	Delete: "In other processes and devices the structures of the present invention may be formed on a portion of a wafer or across substantially all of a wafer."
Column 9, Line 59	Delete: "also formed" Insert: --also be formed--
Column 10, Line 52	Delete: "claim 3 the" Insert: --claim 3 wherein the--
Column 12, Line 9	Delete: "claim 19 the" Insert: --claim 19 wherein the--
Column 12, Line 14	Delete: "wherein wherein" Insert: --wherein--

Signed and Sealed this

Third Day of October, 2006



JON W. DUDAS
Director of the United States Patent and Trademark Office

(12) **United States Patent**
Mears et al.

(10) **Patent No.: US 6,927,413 B2**
(45) **Date of Patent: Aug. 9, 2005**

(54) **SEMICONDUCTOR DEVICE INCLUDING BAND-ENGINEERED SUPERLATTICE**

(75) Inventors: **Robert J. Mears**, Wellesley, MA (US); **Jean Augustin Chan Sow Fook Yiptong**, Waltham, MA (US); **Marek Hytha**, Brookline, MA (US); **Scott A. Kreps**, Southborough, MA (US); **Ilija Dukovski**, Newton, MA (US)

(73) Assignee: **RJ Mears, LLC**, Waltham, MA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 70 days.

(21) Appl. No.: **10/717,375**

(22) Filed: **Nov. 19, 2003**

(65) **Prior Publication Data**

US 2005/0017235 A1 Jan. 27, 2005

Related U.S. Application Data

(63) Continuation of application No. 10/647,060, filed on Aug. 22, 2003, which is a continuation-in-part of application No. 10/603,696, filed on Jun. 26, 2003, and a continuation-in-part of application No. 10/603,621, filed on Jun. 26, 2003.

(51) **Int. Cl.**[7] **H01L 29/06**
(52) **U.S. Cl.** **257/15**; 257/19
(58) **Field of Search** 257/15, 13, 18, 257/19, 29, 97, 77, 628

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Primary Examiner—David Nelms
Assistant Examiner—Thinh T Nguyen
(74) *Attorney, Agent, or Firm*—Allen, Dyer, Doppelt, Milbrath & Gilchrist, P.A.

(57) **ABSTRACT**

A semiconductor device includes a superlattice that, in turn, includes a plurality of stacked groups of layers. The device may also include regions for causing transport of charge carriers through the superlattice in a parallel direction relative to the stacked groups of layers. Each group of the superlattice may include a plurality of stacked base semiconductor monolayers defining a base semiconductor portion and an energy band-modifying layer thereon. Moreover, the energy-band modifying layer may include at least one non-semiconductor monolayer constrained within a crystal lattice of adjacent base semiconductor portions. Accordingly, the superlattice may have a higher charge carrier mobility in the parallel direction than would otherwise be present.

26 Claims, 9 Drawing Sheets